WHAT IS CLAIMED IS:

1. An information handling system comprising:

a CPU operable to process information, the CPU having variable power demands for power supplied within predetermined voltage and current tolerances;

a power supply interfaced with the CPU and operable to provide power to the CPU at the variable power demands within a response time;

one or more capacitors disposed between the power supply and the CPU, the capacitors operable to provide capacitance to buffer current between the power supply and CPU to compensate for power supply response times to current load changes; and

a capacitance feed forward loop interfaced between the capacitors and the CPU and operable to replicate current present in the capacitors and to communicate the replicated current to the power supply with a gain selected to adjust power supply output to fall within the predetermined voltage and current tolerances in a reduced response time.

2. The information handling system of Claim 1 wherein the capacitance feed forward loop comprises a filter having a frequency compensation pole.

3. The information handling system of Claim 2 wherein power is provided to the CPU from the power supply through an equivalent series resistance, the pole canceling the zero created by the equivalent series resistance and the output capacitance.

4. The information handling system of Claim 1 further comprising:

one or more inductors disposed between the power supply and the capacitors;

a current feed back loop communicating compensation to the power supply for current sensed between the inductors and the capacitors; and

a voltage feed back loop communicating compensation to the power supply for voltage sensed at the CPU.

5. A method for supplying power to a microprocessor having variable power demands, the method comprising:

outputting power from a power supply to the microprocessor;

communicating variations in microprocessor power demand to the power supply;

adjusting power output from the power supply in response to the variations in microprocessor power demand within a predetermined response time;

buffering current with capacitors to manage differences between power supplied by the power supply and power demanded by the microprocessor over the response time;

estimating the current present in the capacitors; and

reducing the response time by communicating the estimated current present in the capacitors to the power supply and adjusting power output from the power supply in response to the estimated current present in the capacitors.

6. The method of Claim 5 wherein communicating variations in microprocessor power demand further comprises sensing current output from the power supply and voltage at the microprocessor and communicating the sensed current and voltage to the power supply as gain adjusted compensation signals.

7. The method of Claim 5 wherein the microprocessor comprises an information handling system CPU.

8. The method of Claim 5 wherein estimating the current present in the capacitors further comprises:

sensing the current in the capacitors and the microprocessor;

applying the sensed current to a filter having a pole that cancels a zero created by the equivalent series resistance associated with the power supply and the capacitance associated with the capacitors.

9. The method of Claim 8 wherein reducing the response time further comprises:

applying a gain parameter to the estimated current present in the capacitors to generate a compensation signal;

communicating the compensation signal to the power supply; and

adjusting the power supply output in accordance with the compensation signal.

10. A system for controlling power supplied to a microprocessor having variable power demands, the system comprising:

a power supply operable to output power to the microprocessor to meet the variable demands;

one or more capacitors disposed between the power supply and the microprocessors, the capacitors operable to buffer current during variances of power demanded by the microprocessor to maintain power supplied to the microprocessor within predetermined tolerances;

a capacitance compensation loop operable to sense voltage change across the capacitor, to apply the sensed voltage change to estimate the current of the capacitor, and to determine a compensation signal from the estimate for communication with the power supply to adjust power output.

11. The system of Claim 10 further comprising:

a current compensation loop operable to sense current in the capacitor to determine a current compensation signal for communication with the power supply.

12. The system of Claim 10 further comprising:

a voltage compensation loop operable to sense voltage at the CPU to determine a voltage compensation signal for communication with the power supply.

13. The system of Claim 10 wherein the capacitance compensation loop comprises a feed forward compensation loop.

14. The system of Claim 13 wherein the capacitance compensation loop comprises a frequency filter that replicates current present in the capacitor.

15. The system of Claim 14 wherein the frequency filter comprises a pole positioned in frequency compensation to cancel a zero associated with power supply equivalent series resistance and capacitance.

16. The system of Claim 10 wherein the power supply comprises a multiphase power supply.

17. The system of Claim 10 wherein the power supply comprises a single phase power supply.